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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,241	KOH, PHILIP JOSEPH	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23 - 61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23,25,26-30,34,35,37,40-44,47,50,55,56 and 57* is/are rejected.

7)☒ Claim(s) *24,31-33,36,38,39,45,46,48,49,51-54 and 58-61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 112

1. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 25 recites the limitation "over said aperture." There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 23, and 26 – 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Ball (US 6,337,227).

3. Regarding Claims 23 and 26, Ball discloses a method of making an interconnectable package comprising:

providing a first wafer having a plurality of bottom die (Figures 4 and 5, bottom),

providing a second wafer having a plurality of top die (Figures 4 and 5, top),

patterning at least one "transmission line" (612) (Figure 7) on at least one side of said bottom die of said first wafer,

etching at least one integral connector and at least one "transmission line" (626) on said top die of second wafer,

coupling a component (integrated circuit elements) to each of said plurality of bottom die of said first wafer,

forming a wafer stack by bonding said second wafer (202) to said first wafer (204) (Figure 2) such that said top die of said second wafer is aligned with said bottom die of said first wafer (Col. 6, lines 22 – 30), and

dicing said wafer stack into a plurality of individual packets (Figure 5) wherein each of said plurality of packets contains a top die bonded to said bottom die, wherein the top die has an integral connector (626) and the bottom die has a component (integrated circuit element).

4. Regarding Claims 27 – 29, Ball discloses components or "devices" (Col. 1, lines 15 – 18) that encompass all of the well known semiconductor devices recited in Claims 27 – 29.

5. Regarding Claim 30, Ball discloses a method of making an interconnectable package, where-in the integral connector on top of the die on second wafer is shaped as a male connection component (Figure 7) (626,610).

6. Claims 34, 35, 37, 40 – 44, 47, 50, and 55 – 57 are rejected under 35 U.S.C. 102(e) as being anticipated by Hikita et al. (6,717,244 B1).

7. Regarding Claim 34, Hikita et al. disclose a method of making a dielectric package for housing a component comprising:

providing a first die (2a) (Figure 1) comprising a first integral planar connection member having a first planar conductor (4) patterned thereon,

providing a second die (1) comprising a second planar conductor (3) patterned on said second die, and

bonding said second die to said first die to said first die such that an outermost planar surface of the first planar conductor is placed in planar contact with outermost planar surface of the second planar conductor, thus forming said dielectric package (Figures 3A, 3B) (Col. 4, line 66 through Col. 5, line 5).

8. Regarding Claim 35, Hikita et al. disclose that the first integral planar connection member (4) is formed having a male shape (Figure 1).

9. Regarding Claims 37 and 57, Hikita et al. disclose a method of making a dielectric package for housing a component, further comprising coupling a component to the first die prior to the bonding of the second die to the first die (See Figure 3A).

10. Regarding Claim 40, Hikita et al. disclose a method for making a dielectric package for housing a component, wherein the component is an integrated circuit (chip) (Col. 1, lines 10 – 15).

11. Regarding Claims 41 - 43, Hikita et al. discloses components or "devices" (Col. 1, lines 10 – 15) that encompass all of the well known semiconductor devices recited in Claims 41 – 43.

12. Regarding Claim 44, Hikita et al. disclose a method of making a dielectric package, wherein the dielectric package has a plurality of integral planar connection members (See Figure 1).

13. Regarding Claim 47, Hikita et al. disclose a method of making a dielectric package for housing a component, wherein the bonding of the second die to the first die further comprises aligning the first integral planar connection member on the first die to a second integral planar connection member on the second die whereupon the second planar conductor is provided (Col. 3, lines 23 – 30).

14. Regarding Claim 50, Hikita et al. disclose a method of making a dielectric package for housing a component, wherein the first and second planar conductors are at least partially held in the planar contact by a resilient member (52) (Figure 3A) (Col. 4, lines 57 – 65).

15. Regarding Claim 55, Hikita et al. disclose a method of making a dielectric package for housing a component, wherein a plurality of the first planar conductors are patterned on the first

integral connection member separated by non-conductive portions (See Figure 1)

16. Regarding Claim 56, Hikita et al. disclose a method of making a dielectric package for housing a component, wherein a plurality of the second planar conductors are patterned on the second die to correspond with the plurality of first planar conductors (See Figure 1)

Claim Objections

17. Claims 24 and 31 – 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

A review of the prior art shows that in the claims of the instant application, the method of making an interconnectable package comprising *"etching an aperture in said top die of said second wafer such that said component may be placed through said aperture and coupled to said bottom die of said second wafer after the bonding and dicing of said first and second wafer,"* or an integral connector shaped as a *"hermaphrodite connection"* or a "*female connection"* is not taught or suggested in the art.

18. Claims 36, 38, 39, 45, 46, 48, 49, 51 – 54, and 58 – 61 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in in5ependent form including all of the limitations of the base claim and any intervening claims.

A review of the prior art shows that in the claims of the instant application, the method of making an interconnectable package comprising *"etching an aperture into said second die, "wherein the component is placed through said aperture on said second die and coupled to the first die,"* and where the *"integral planar connection members comprise both female and male shaped connection members,"* is not taught or suggested in the art.

Response to Arguments

19. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusions

20. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
October 19, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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